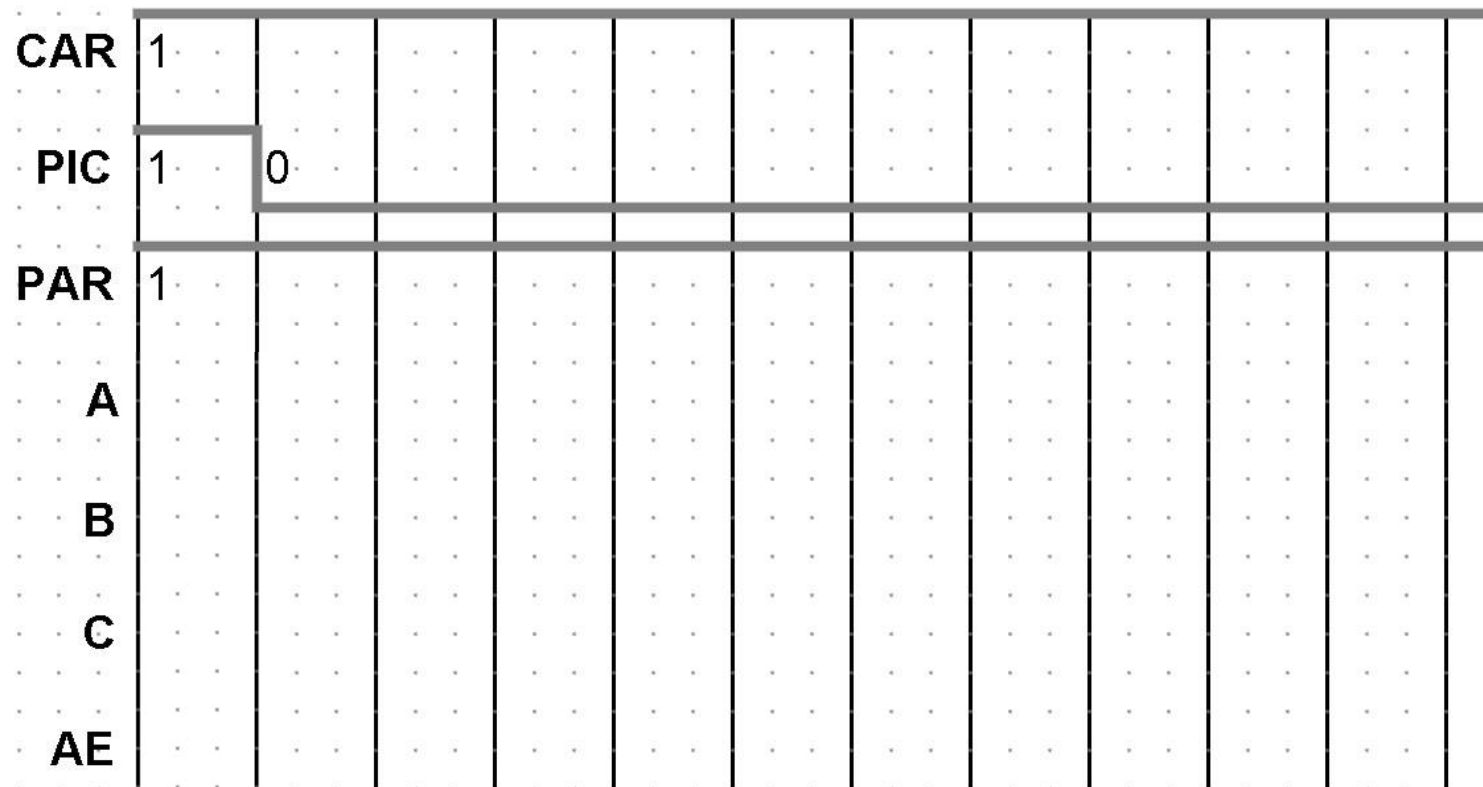
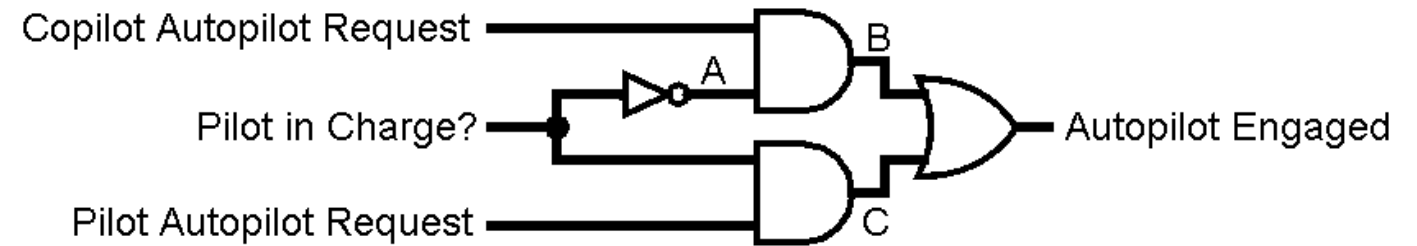


# 1. Circuit Timing Behavior

- Assume 1 ns (3 tick) delay for all gates



## 2. K-map Example: Majority Circuit

- Filling in a Karnaugh map:

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

| AB |   | 00 | 01 | 11 | 10 |
|----|---|----|----|----|----|
| C  | 0 |    |    |    |    |
|    | 1 |    |    |    |    |

- Each row of truth table corresponds to ONE cell of Karnaugh map
- Note the jump when you go from input 011 to 100  
(*most mistakes made here*)

# General K-map Rules

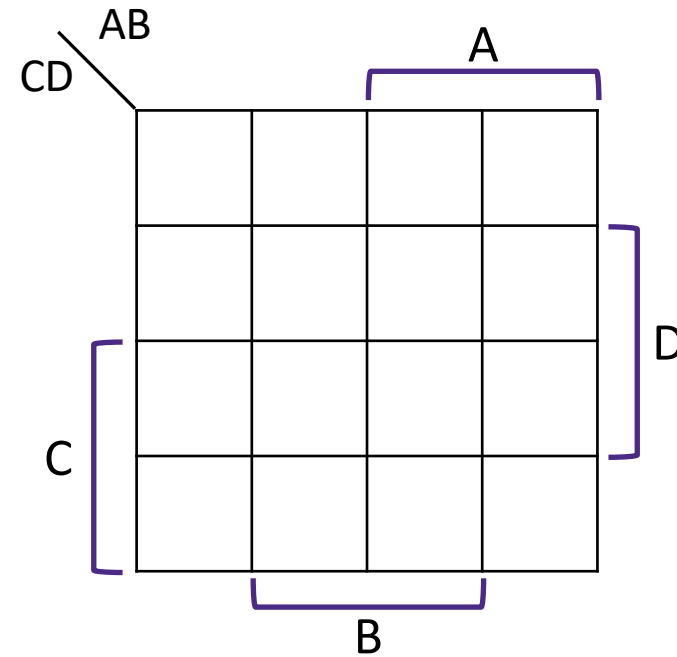
- Only group in powers of 2
  - Grouping should be of size  $2^i \times 2^j$
  - Applies for both directions
- Wraps around in all directions
  - “Corners” case is extreme example
- Always choose largest groupings possible
  - Avoid single cells whenever possible
- $F = BD + \overline{B}\overline{D} + ACD$

|    |    |    |    |    |    |
|----|----|----|----|----|----|
|    | AB | 00 | 01 | 11 | 10 |
| CD | 00 | 1  | 0  | 0  | 1  |
|    | 01 | 0  | 1  | 1  | 0  |
|    | 11 | 0  | 1  | 1  | 1  |
|    | 10 | 1  | 0  | 0  | 1  |

- 1) NOT a valid group
- 2) IS a valid group
- 3) IS a valid group
- 4) “Corners” case
- 5) 1 of 2 good choices here

### 3. K-Map Example

- $F = \overline{A}D + BD + \overline{B}C + A\overline{B}D$



## 4. Don't Cares

- Use symbol 'X' to mean it can be either a 0 or 1
  - Make choice to simplify final expression

| CD \ AB | A |   |   |   |
|---------|---|---|---|---|
|         | 0 | 0 | X | 0 |
| C       | 1 | 1 | X | 1 |
|         | 1 | 1 | 0 | 0 |
|         | 0 | X | 0 | 0 |
| B       |   |   |   | D |

Let all X = 0:

F =

| CD \ AB | A |   |   |   |
|---------|---|---|---|---|
|         | 0 | 0 | X | 0 |
| C       | 1 | 1 | X | 1 |
|         | 1 | 1 | 0 | 0 |
|         | 0 | X | 0 | 0 |
| B       |   |   |   | D |

Let all X = 1:

F =

| CD \ AB | A |   |   |   |
|---------|---|---|---|---|
|         | 0 | 0 | X | 0 |
| C       | 1 | 1 | X | 1 |
|         | 1 | 1 | 0 | 0 |
|         | 0 | X | 0 | 0 |
| B       |   |   |   | D |

Choose wisely:

F =

## 5. Design Example: 2-bit Adder

**K-map for X**

|         |   |   |   |   |   |
|---------|---|---|---|---|---|
| CD \ AB |   | A |   |   |   |
|         |   | 0 | 0 | 0 | 0 |
| C       | 0 | 0 | 0 | 1 | 0 |
|         | 1 | 0 | 1 | 1 | 1 |
|         | D | 0 | 0 | 1 | 1 |
|         |   | B |   |   |   |

**K-map for Y**

|         |   |   |   |   |   |
|---------|---|---|---|---|---|
| CD \ AB |   | A |   |   |   |
|         |   | 0 | 0 | 1 | 1 |
| C       | 0 | 0 | 1 | 0 | 1 |
|         | 1 | 1 | 0 | 1 | 0 |
|         | D | 1 | 1 | 0 | 0 |
|         |   | B |   |   |   |

**K-map for Z**

|         |   |   |   |   |   |
|---------|---|---|---|---|---|
| CD \ AB |   | A |   |   |   |
|         |   | 0 | 1 | 1 | 0 |
| C       | 0 | 1 | 0 | 0 | 1 |
|         | 1 | 1 | 0 | 0 | 1 |
|         | D | 0 | 1 | 1 | 0 |
|         |   | B |   |   |   |

X =

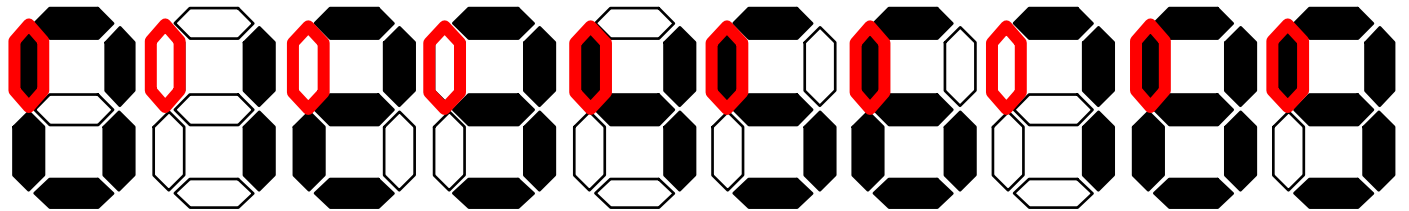
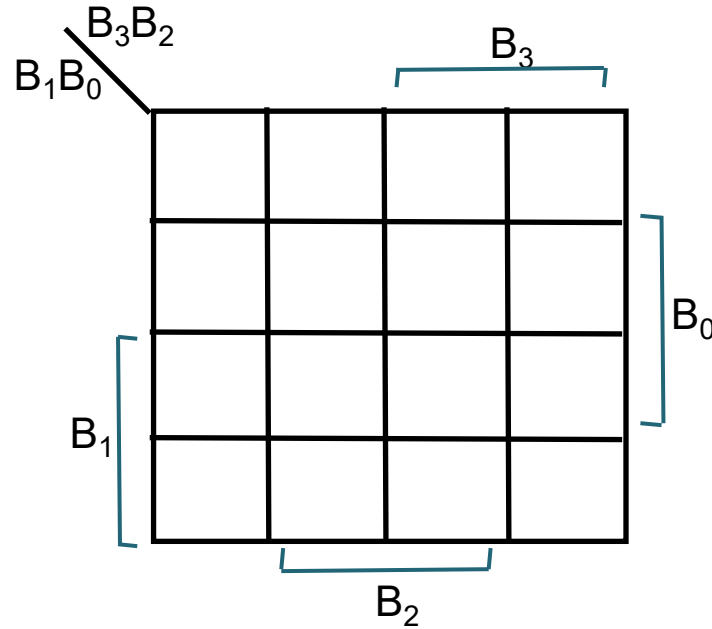
Y =

Z =

## 6. Case Study: Seven-Segment Display

- Implement **L5**:

| B3 | B2 | B1 | B0 | L5 |
|----|----|----|----|----|
| 0  | 0  | 0  | 0  | 1  |
| 0  | 0  | 0  | 1  | 0  |
| 0  | 0  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 0  |
| 0  | 1  | 0  | 0  | 1  |
| 0  | 1  | 0  | 1  | 1  |
| 0  | 1  | 1  | 0  | 1  |
| 0  | 1  | 1  | 1  | 0  |
| 1  | 0  | 0  | 0  | 1  |
| 1  | 0  | 0  | 1  | 1  |



## 7. 7-Seg Display in Verilog

```
module seg7 (bcd, leds);  
    input  logic [3:0] bcd;  
    output logic [6:0] leds;  
  
    always_comb  
        case (bcd)  
            // 3210           6543210  
            4'b0000: leds = 7'b0111111;  
            4'b0001: leds = 7'b0000110;  
            4'b0010: leds = 7'b1011011;  
            4'b0011: leds = 7'b1001111;  
            4'b0100: leds = 7'b1100110;  
            4'b0101: leds = 7'b1101101;  
            4'b0110: leds = 7'b1111101;  
            4'b0111: leds = 7'b0000111;  
            4'b1000: leds = 7'b1111111;  
            4'b1001: leds = 7'b1101111;  
            default: leds = 7'bX;  
        endcase  
    endmodule
```